

Technical Data  
Datasheet 6132, Rev. -

## SiC FET Full Bridge with Integrated Gate Drive

### FEATURES:

- 1200VDC max voltage
- 60A max current
- Compact package
- Temperature range -55°C to +125°C
- Efficient conduction cooled design
- Total weight: 1.10 oz.



### DESCRIPTION:

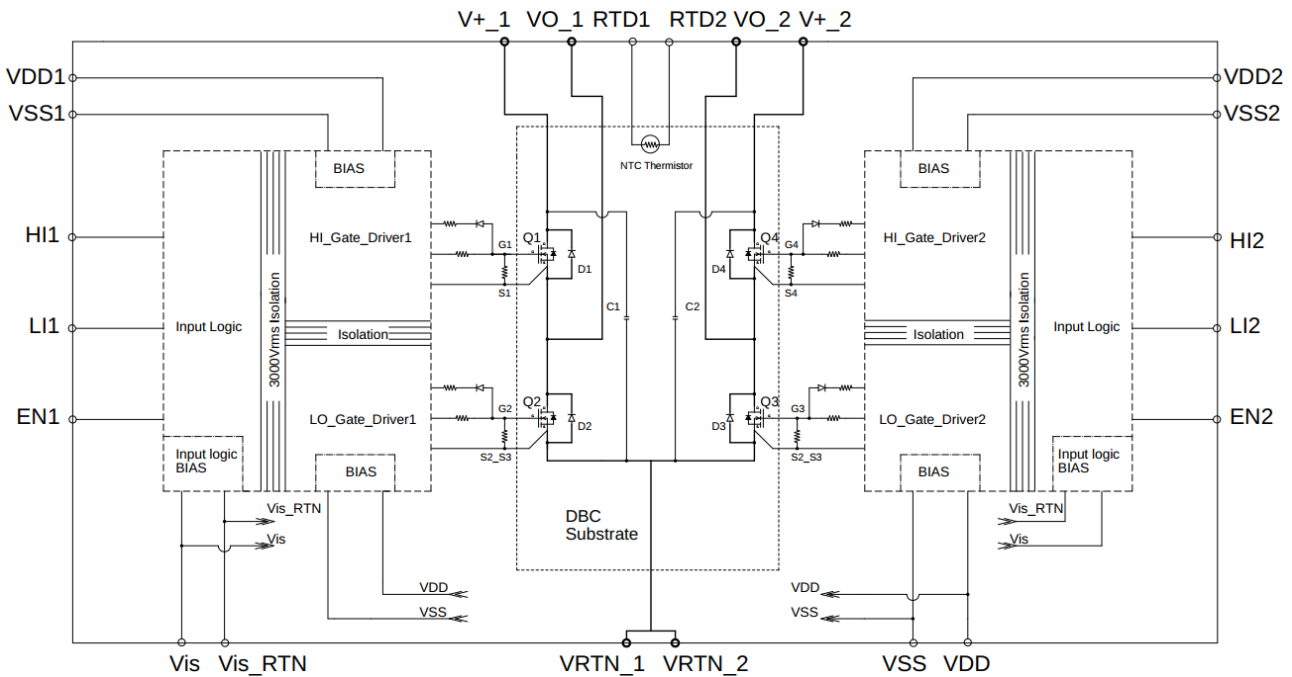
This SiC FET Full Bridge power module can be used in various applications including, but not limited to, power converters and motor drives. The integrated gate drive simplifies the system design and optimizes the dynamic performance of the bridge.

The small size of this complete module makes it ideal for high reliability industrial, aerospace, and military applications.

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Bus Supply Voltage			1200	V
PWM Switching Frequency	$F_{SW}$	-	500	kHz
Continuous Drain Current, each Leg of Full Bridge	$I_D$	-	60	A
Pulsed Drain Current, each Leg of Full Bridge Pulse Width limited by $T_{jmax}$	$I_{D(pulse)}$	-	120	A
Junction Temperature	$T_{jmax}$	-55	150	°C
Storage Temperature	$T_{smax}$	-55	150	°C
Operating Temperature on Cold Plate	$T_{cmax}$	-55	125	°C

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**Figure 1 – Block Diagram**

**Connections for Full Bridge Application**

V+ <sub>1</sub> , V+ <sub>2</sub> :	both pins must connect to DC Bus power supply's Positive, no internal connection between these two pins
VRTN <sub>1</sub> , VRTN <sub>2</sub> :	both pins must connect to DC Bus power supply's Return, VRTN <sub>1</sub> and VRTN <sub>2</sub> are internally tied together
VO <sub>1</sub> , VO <sub>2</sub> :	output connections
HI1, LI1, HI2, LI2:	gate control inputs; internally bypassed to V <sub>is_RTN</sub> with 1.0kohm resistor and 22pF capacitor, external in-line resistors [33ohm, 59ohm] recommended
EN1, EN2:	enable driver outputs; internally bypassed to V <sub>is_RTN</sub> with 1.0kohm resistor and 1nF capacitor, external in-line resistors [33ohm, 59ohm] recommended
Vis /V <sub>is</sub> , V <sub>is_RTN</sub> :	power supply input to logic circuitry
VDD /VDD, VSS:	power supply input to LO_Gate_Driver1 and LO_Gate_Driver2 circuitry
VDD1 /VDD1, VSS1:	power supply input HI_Gate_Driver1 circuitry
VDD2 /VDD2, VSS2:	power supply input for HI_Gate_Driver2 circuitry
RTD1, RTD2	connection to internal thermistor

- Requirements to DC Bus power supply, |V<sub>is</sub>|, |VDD|, |VDD1| and |VDD2|:  
 Minimum 2000VDC isolation between |VDD|, |VDD1| and |VDD2|  
 Minimum 2000VDC isolation between |VDD1|/|VDD2| power supplies and DC Bus power supply.  
 Power supply to |VDD| needs to be isolated to DC Bus power supply: VSS is internally clamped 3.6V below VRTN<sub>1</sub>/VRTN<sub>2</sub>, for negative gate drive  
 3000VRMS isolation between power supply to |V<sub>is</sub>| and DC Bus/|VDD1|/|VDD2| power supplies is recommended

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**ELECTRICAL CHARACTERISTICS OF FULL BRIDGE, PER EACH LEG**

$T_J = 25^\circ\text{C}$ , UNLESS OTHERWISE SPECIFIED.

Production units are tested at room temperature. Low/High temperature operation is guaranteed by design.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V+ <sub>1</sub> , V+ <sub>2</sub>	DC Bus Supply Voltage, to V <sub>RTN1</sub> , V <sub>RTN_2</sub>		- 400	1200 600	VDC
<b>MOSFET (Q1, Q2, Q3, Q4) Characteristics</b>					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage I <sub>D</sub> = 100 $\mu$ A, V <sub>GS</sub> = 0V	1200			VDC
I <sub>D</sub>	Continuous Drain Current T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C			60 30	A
I <sub>D(pulse)</sub>	Pulsed Drain Current			120	A
V <sub>GS</sub>	Gate to Source Voltage		-4/+15 Static	-8/+19 Dynamic	VDC
I <sub>GSS</sub>	Gate-Source Leakage Current V <sub>GS</sub> = +15V, V <sub>DS</sub> = 0V		10	250	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage I <sub>D</sub> = 17.7mA, V <sub>DS</sub> = V <sub>GS</sub>	1.8 -	2.5 2.0	3.6 -	VDC
I <sub>DSS</sub>	Zero Gate Voltage Drain Current V <sub>DS</sub> = 1200 V, V <sub>GS</sub> = 0V	-	1	25	$\mu$ A
R <sub>DS(on)</sub>	Drain-Source On-State Resistance I <sub>D</sub> = 50A, V <sub>GS</sub> = +15V	14 -	22 40	30 -	m $\Omega$
C <sub>ISS</sub> C <sub>OSS</sub> C <sub>RSS</sub>	Input Capacitance Output Capacitance Reverse Transfer capacitance V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, f = 100 kHz, V <sub>AC</sub> = 25 mV		4820 300 18		pF
Q <sub>gs</sub> Q <sub>gd</sub> Q <sub>g</sub>	Gate to Source Charge Gate to Drain Charge Total Gate Charge V <sub>DS</sub> = 600 V, I <sub>D</sub> = 50A, V <sub>GS</sub> = -4V/+15V		49 50 162		nC
<b>Anti-parallel Diode (D1, D2, D3, D4) Characteristics</b>					
V <sub>F</sub>	Diode Forward Voltage I <sub>F</sub> = 20A	1.0 -	1.5 2.0	1.8 -	VDC
I <sub>R</sub>	Reverse Current V <sub>R</sub> = 1200V	-	35	200	$\mu$ A
QC	Total Capacitive Charge I <sub>F</sub> = 20A, V <sub>R</sub> = 400V, di/dt = 150 A/ $\mu$ s	-	68	-	nC
<b>Internal DC Link - Snubber Capacitance between V+<sub>1</sub>/V+<sub>2</sub> and VRTN<sub>1</sub>/VRTN<sub>2</sub></b>					
C1, C2	1.2 kV, NP0, $\pm$ 5%, -55°C to 150°C	-	12	-	nF
<b>Stray inductance</b>					
L <sub>stray</sub>	between pin 1 and 3 or pin 7 and 6		7.0		nH

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**ELECTRICAL CHARACTERISTICS OF LOGIC AND DRIVER INPUT**

T<sub>J</sub>=25°C, UNLESS OTHERWISE SPECIFIED.

Production units are tested at room temperature. Low/High temperature operation is guaranteed by design.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
<b>Absolute Maximum Ratings</b>					
V <sub>is</sub>	Logic supply voltage, V <sub>is</sub> to V <sub>is_RTN</sub>	-0.5		20.0	VDC
HI1, LI1, HI2, LI2	Input logic signals to V <sub>is_RTN</sub> , TTL/CMOS compatible input threshold	-0.5		V <sub>Vis</sub> +0.5	VDC
VDD, VSS VDD1, VSS1 VDD2, VSS2	Driver side supply voltage	-0.5		22.0	VDC
<b>Recommend Operating Conditions</b>					
V <sub>is</sub>	Logic supply voltage, V <sub>is</sub> to V <sub>is_RTN</sub>	3.0		15.0	VDC
VDD, VSS VDD1, VSS1 VDD2, VSS2	Driver side supply voltage	18.0		20.0	VDC
<b>V<sub>is</sub> to V<sub>is_GND</sub> Undervoltage Thresholds</b>					
V <sub>is_ON</sub>	UVLO rising threshold	2.5	2.7	2.9	VDC
V <sub>is_OFF</sub>	UVLO falling threshold	2.3	2.5	2.7	VDC
V <sub>is_HYS</sub>	UVLO threshold hysteresis		0.2		VDC
<b>VDD-VSS, VDD1-VSS1, VDD2-VSS2 Undervoltage Thresholds</b>					
	UVLO rising threshold	12.5	13.5	14.5	VDC
	UVLO falling threshold	11.5	12.5	13.5	VDC
	UVLO threshold hysteresis		1.0		VDC
<b>EN1, EN2 Thresholds</b>					
V <sub>ENH</sub>	Enable high voltage	2.0			VDC
V <sub>ENH</sub>	Enable low voltage			0.8	VDC
<b>HI1, LI1, HI2 and LI2 Thresholds</b>					
	Input logic high threshold voltage	1.6	1.8	2.0	VDC
	Input logic low threshold voltage	0.8	1.0	1.2	VDC
	Input logic threshold hysteresis		0.8		VDC
<b>Switching Characteristics (V<sub>is</sub> = 5V, VDD/VDD1/VDD2 = 15V)</b>					
t <sub>RISE</sub>	Output rise time, 20% to 80%, 1.8nF capacitor at gate drive output		6	16	ns

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SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t <sub>FALL</sub>	Output fall time, 90% to 10%, 1.8nF capacitor at gate drive output		7	12	ns
t <sub>PDHL</sub>	Propagation delay from logic input to gate drive signal falling edges	14	19	30	ns
t <sub>PDLH</sub>	Propagation delay from logic input to gate drive signal rising edges	14	19	30	ns
t <sub>PWD</sub>	Pulse width distortion  t <sub>PDLH</sub> - t <sub>PDHL</sub>			5	ns
t <sub>DM</sub>	Propagation delays matching between V <sub>G1</sub> and V <sub>G2</sub> , V <sub>G3</sub> and V <sub>G4</sub>			5	ns
<b>NTC Thermistor Characteristics (Heraeus Nexensos's M Sensor)</b>					
R <sub>0</sub>	Resistance @ T <sub>C</sub> = 0 °C		1		K Ohm
R <sub>TOL</sub>	Resistance Tolerance			±0.12	%
	Measuring Current	0.1		0.3	mA
TCR	$TCR = \frac{R_{100} - R_0}{R_0 * 100^\circ C}$ R <sub>100</sub> is resistance at 100°C, R <sub>0</sub> is resistance at 0°C		3850		ppm/K
	Temperature Range	-70		500	°C
Resistance vs Temperature	$t \geq 0^\circ$ $R(t) = R_0 * (1 + A * t + B * t^2)$ $t < 0^\circ C$ $R(t) = R_0 * (1 + A * t + B * t^2 + C * (t - 100^\circ C) * t^3)$ ;		$A = 3.9083 * 10^{-3}$ $B = -5.775 * 10^{-7}$ $C = -4.183 * 10^{-12}$	$^\circ C^{-1}$ $^\circ C^{-2}$ $^\circ C^{-4}$	
<b>Internal Configurations</b>					
VSS-VRTN_1 VSS-VRTN_2	VSS is internally clamped below VRTN_1/VTRN_2 for negative gate drive		-3.6		VDC
DT	Internal dead time setting		No		

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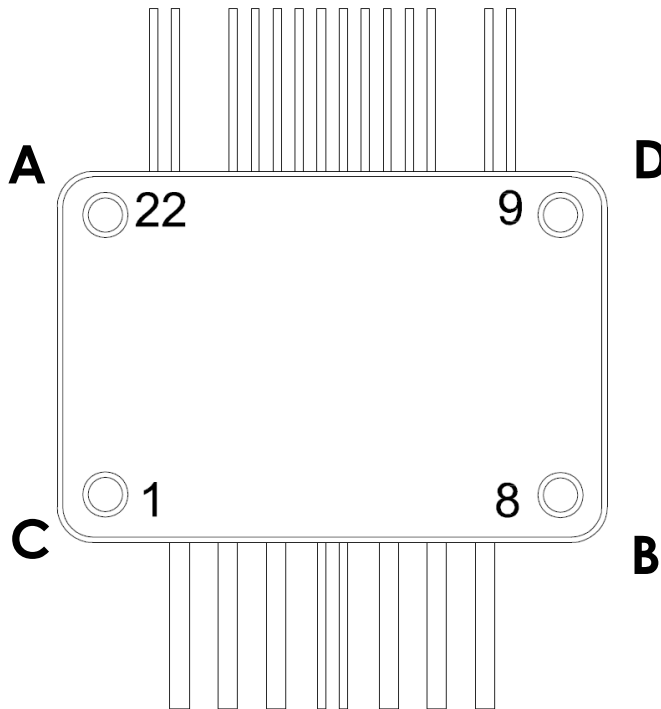
**THERMAL AND MECHANICAL CHARACTERISTICS**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
R <sub>θJB_M</sub>	MOSFET Junction-to- Base Plate Thermal Resistance Per Leg	-	.339	.390	°C/W
R <sub>θJB_D</sub>	Diode Junction-to-Base Plate Thermal Resistance Per Leg	-	.884	1.017	°C/W
Isolations	All pins to Base Plate/Screw mounting pads	-	-	2500	VDC
	Logic signals to driver signals	$ V_{is}-VDD $ $ V_{is}-VDD1 $ $ V_{is}-VDD2 $	-	2500	V <sub>RMS</sub>
Mounting Torque	<b>see installation instructions</b> #4 Size Screw	3	-	4	in-lbs.
	Weight Module	-	32	40	g

**INSTALLATION INSTRUCTIONS:**

Recommended thermal interface material = Laird Tgon 805 (5 mil thick graphite pad)

1. Fasten screws to 1 to 2 in-lb. of torque in the following sequence: A, B, C, D.
2. Fasten screws to final torque in the same sequence: A, B, C, D



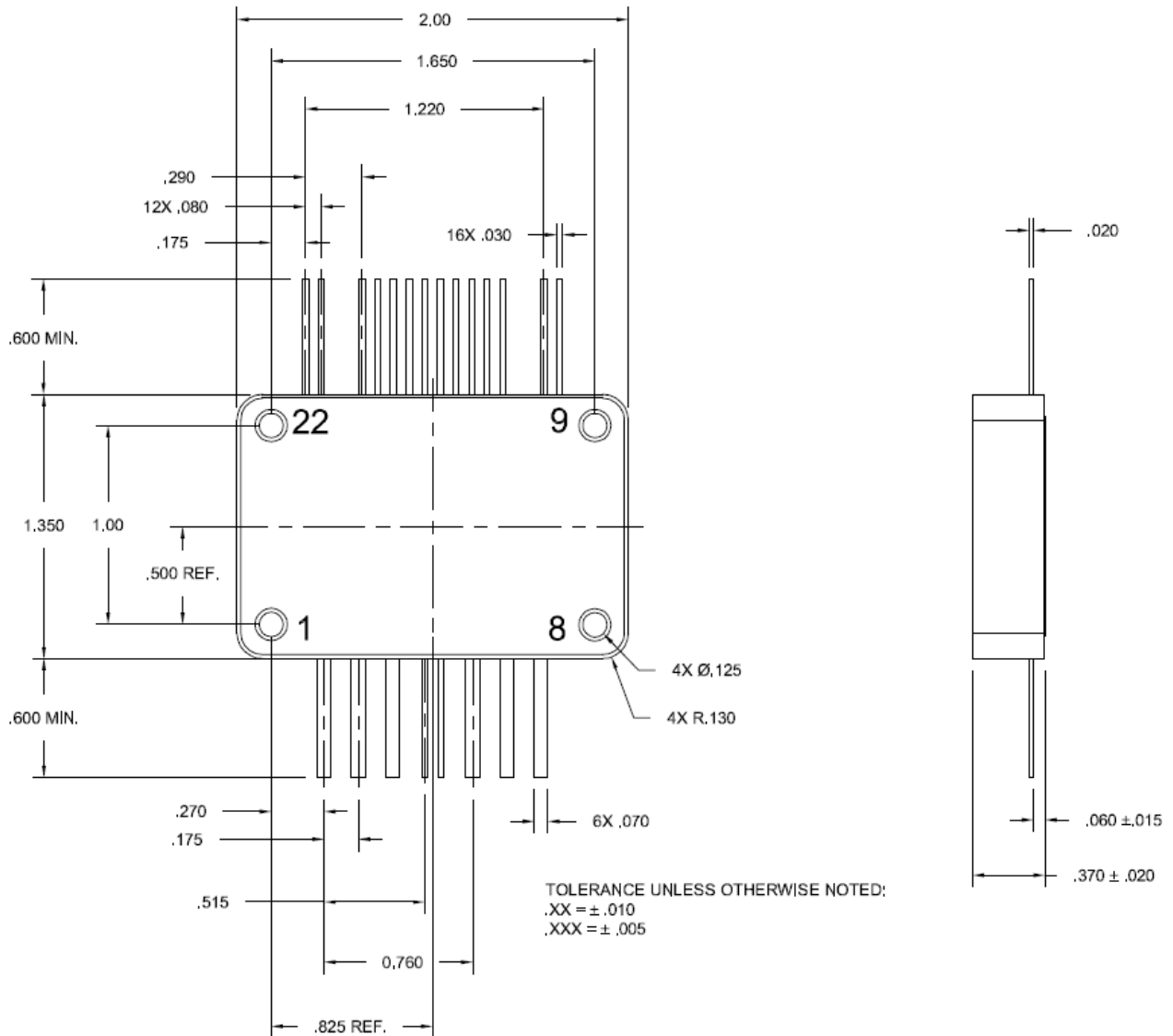
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**PART NUMBER DESCRIPTION:**

- "SPG060C120P2" – Straight Leads
- "SPG060C120P2A" – Surface Mount Lead Formation

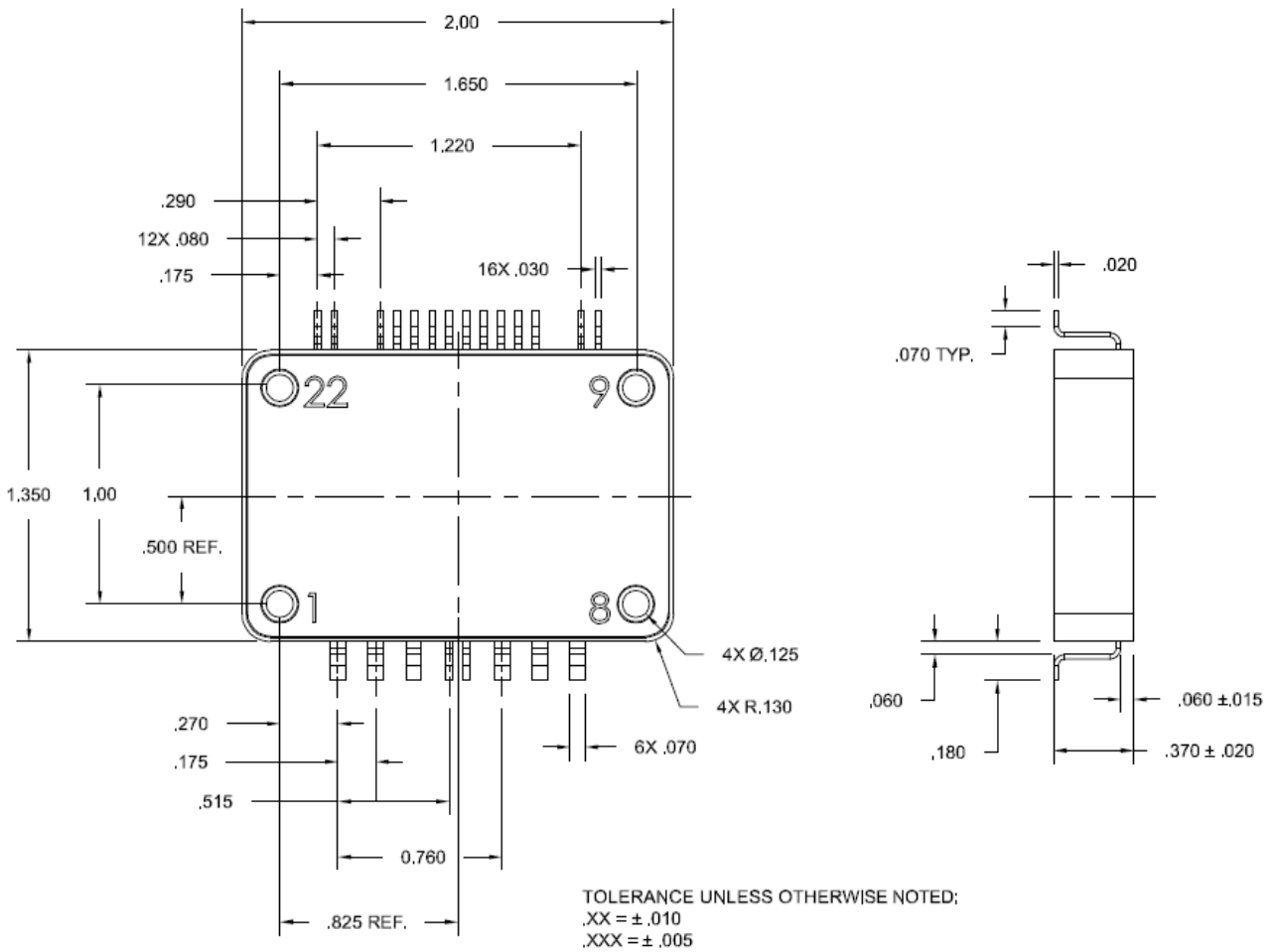
**MECHANICAL OUTLINES (inches)**

**SPG060C120P2**



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**SPG060C120P2A**



**PINOUTS**

- |               |                 |
|---------------|-----------------|
| Pin 1: V+_1   | Pin 9: VSS2     |
| Pin 2: VO_1   | Pin 10: VDD2    |
| Pin 3: VRTN_1 | Pin 11: HI2     |
| Pin 4: VDD    | Pin 12: LI2     |
| Pin 5: VSS    | Pin 13: EN2     |
| Pin 6: VRTN_2 | Pin 14: Vis     |
| Pin 7: VO_2   | Pin 15: RTD1    |
| Pin 8: V+_2   | Pin 16: RTD2    |
|               | Pin 17: Vis_RTN |
|               | Pin 18: LI1     |
|               | Pin 19: HI1     |
|               | Pin 20: EN1     |
|               | Pin 21: VSS1    |
|               | Pin 22: VDD1    |



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