micross components
transforming specialty electronics

# MYX4DDR364M16JT

## 64M16 DDR3 SDRAM - 96 PBGA

Advanced information. Subject to change without notice.

## Features

- Tin-lead ball metalurgy
- Part number MYX4DDR364M16JT-XIT
- $V_{DD}$ = $V_{DDQ}$ = 1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- POSTED CAS ADDITIVE latency (AL)
- Programmable CAS WRITE latency (CWL) based on $_{t}$CK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- $T_C$ of 0°C to 95°C
  - 64ms, 8192 cycle refresh at 0°C to 85°C
  - 32ms, 8192 cycle refresh at 85°C to 95°C
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

| Options | Marking |
|---|---|
| • Configuration | |
| * 64M x 16 | 64M16 |
| • FPGA package (Sn63 Pb37 solder) - x16 | |
| * 96-ball (8mm x 14mm) | JT |
| • Timing - cycle time | |
| * 1.5ns @ CL = 9 (DDR3-1333) | -15 |
| * 1.87ns @ CL = 7 (DDR3-1066) | -18 |
| • Operating temperature | |
| * Commercial (0°C ≤ $T_C$ ≤ +95°C) | None |
| * Industrial (-40°C ≤ $T_C$ ≤ +95°C) | IT |

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AS9100 Rev. C REGISTERED

Table 1: Key Timing Parameters

| Speed Grade | Data Rate (MT/s) | Target $_{t}$RCD-$_{t}$RP-CL | $_{t}$RCD (ns) | $_{t}$RP (ns) | CL (ns) |
|---|---|---|---|---|---|
| -15* | 1333 | 9-9-9 | 13.5 | | |
| -18 | 1066 | 7-7-7 | 13.1 | | |

*Backward compatible to 1066, CL=7

Figure 1: 96-Ball FBGA (Top View), JT

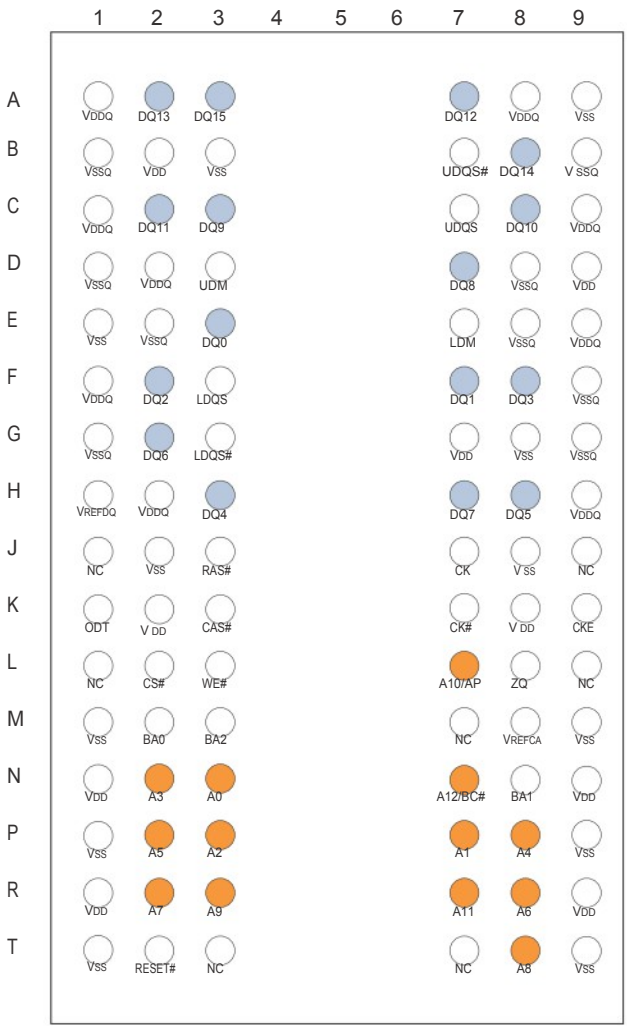
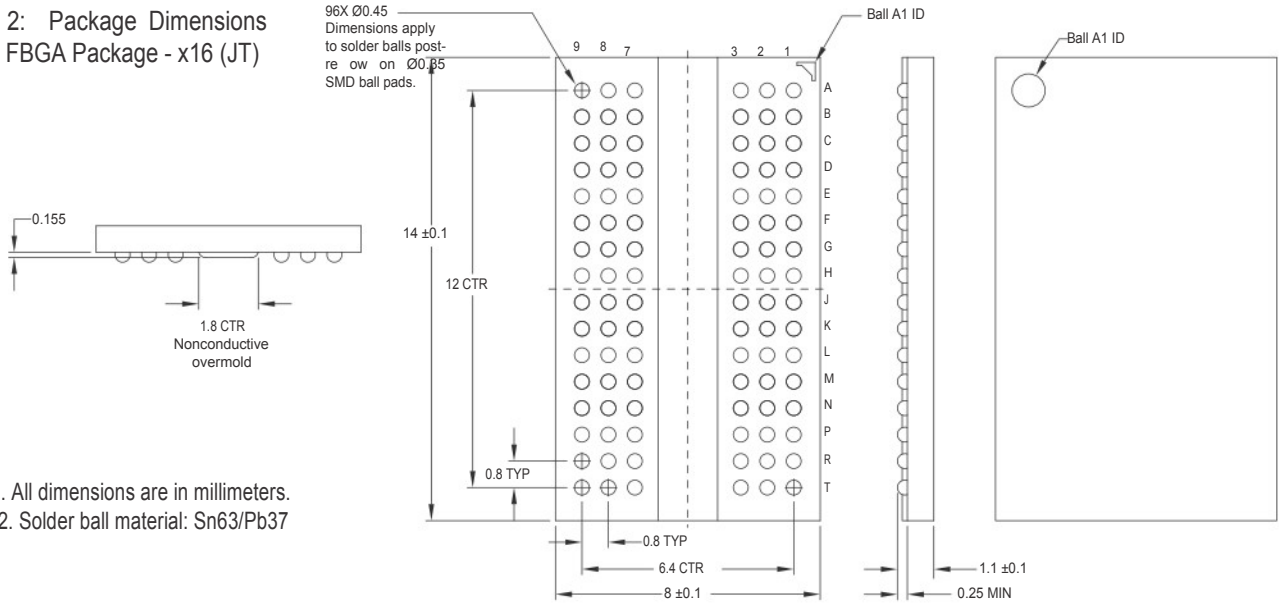



Figure 2: Package Dimensions
96-Ball FBGA Package - x16 (JT)




Notes: 1. All dimensions are in millimeters.
2. Solder ball material: Sn63/Pb37