micross components
transforming specialty electronics

MYX4DDR264M16HW

64M16 DDR2 SDRAM - 84 PBGA

Advanced information. Subject to change without notice.

- Tin-lead ball metalurgy
- Part number MYX4DDR264M16HW-XIT
- V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 $_tCK$
- Selectable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Supports JEDEC clock jitter specification

Options	Marking
• Configuration	
64M x 16 (8M x 16 x 8 banks)	64M16
• FPGA package (Sn63 Pb37) - x16	
84-ball FPGA (8mm x 12.5mm)	HW
• Timing - cycle time	
2.5ns @ CL = 5 (DDR2-800)	-25E
2.5ns @ CL = 6 (DDR2-800)	-25
3.0ns @ CL = 5 (DDR2-667)	-3
• Self refresh	
Standard	None
Low-power	L
• Operating temperature	
Commercial (0°C ≤ T_C ≤ +85°C)	None
Industrial (-40°C ≤ T_C ≤ +95°C; -40°C ≤ T_A ≤ +85°C;)	IT

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Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)					$_tRC$ (ns)
	CL=3	CL=4	CL=5	CL=6	CL=7	
-25E	400	533	800	800	NA	55
-25			667			
-3				NA		

Figure 1: 84-Ball FBGA - x16 Ball Assignments (Top View), 1Gb, HW

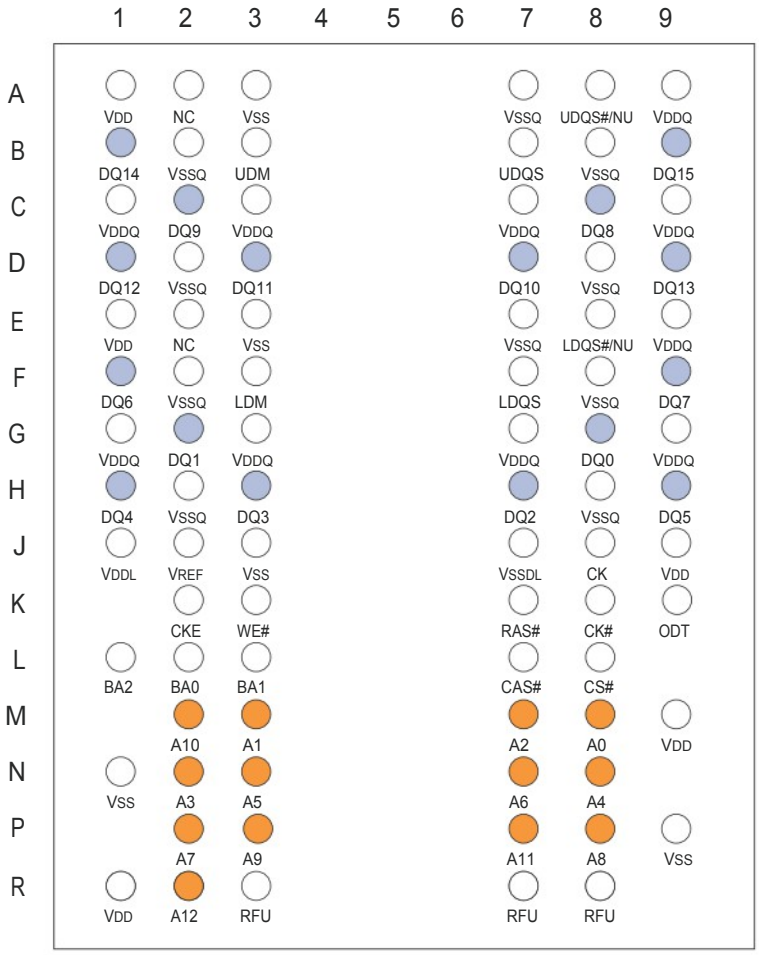
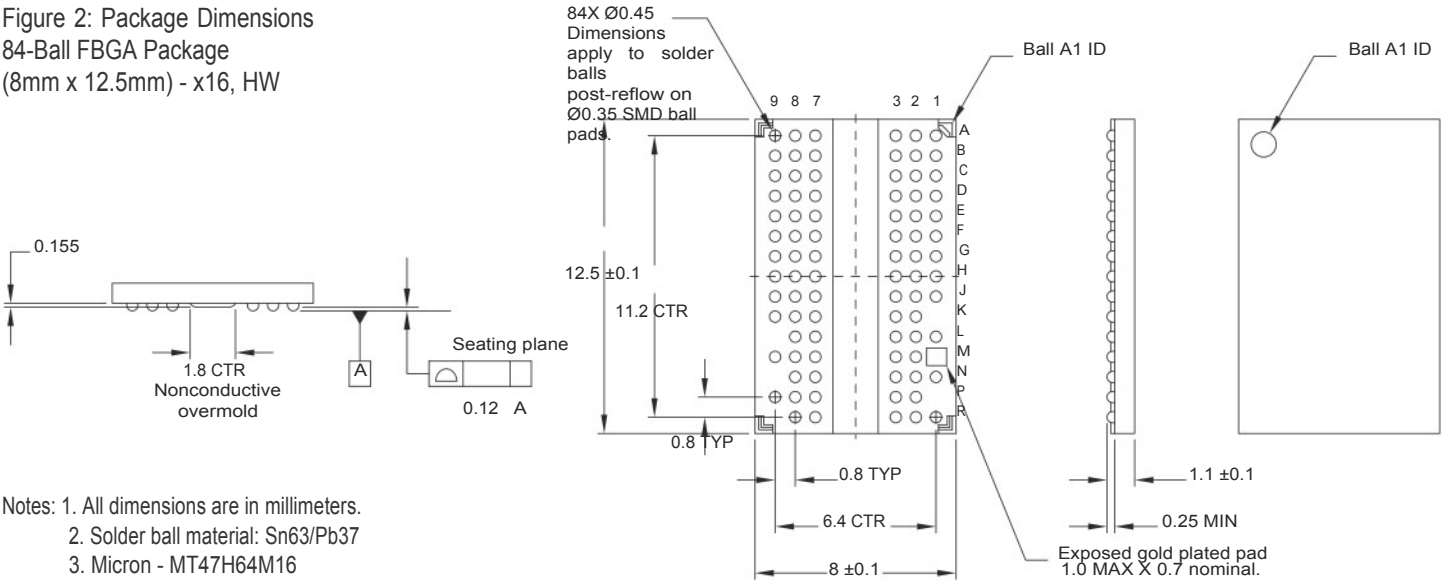


Figure 2: Package Dimensions
84-Ball FBGA Package
(8mm x 12.5mm) - x16, HW



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: Sn63/Pb37
3. Micron - MT47H64M16