

128M16 DDR2 SDRAM - 84 PBGA

Advanced information. Subject to change without notice.

Features

- Tin-lead ball metalurgy
- Part number MYX4DDR2128M16PK-XIT
- $V_{DD} = 1.8V \pm 0.1V$, $V_{DDQ} = 1.8V \pm 0.1V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 tCK
- Selectable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT)
- Supports JEDEC clock jitter specification

Options	Marking
• Configuration	
* 128M x 16 (16M x 16 x 8 banks) 128M16	
• FPGA package (Sn63 Pb37) - x16	
* 84-ball FPGA (9mm x 12.5mm) Rev. C	PK
• Timing - cycle time	
* 2.5ns @ CL = 5 (DDR2-800)	-25E
* 2.5ns @ CL = 6 (DDR2-800)	-25
* 3.0ns @ CL = 5 (DDR2-667)	-3
• Operating temperature	
* Commercial ($0^{\circ}C \leq T_c \leq +85^{\circ}C$)	None
* Industrial ($-40^{\circ}C \leq T_c \leq +95^{\circ}C$; $-40^{\circ}C \leq T_A \leq +85^{\circ}C$;))	IT

AS9100 Rev. C
REGISTERED

MICROSS COMPONENTS
QML
CERTIFIED

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)					tRC (ns)
	CL=3	CL=4	CL=5	CL=6	CL=7	
-25E	400	533	800	800	NA	55
-25			667			
-3			NA			

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Figure 1: 84-Ball FBGA - x16 Ball Assignments (Top View), 2Gb, PK

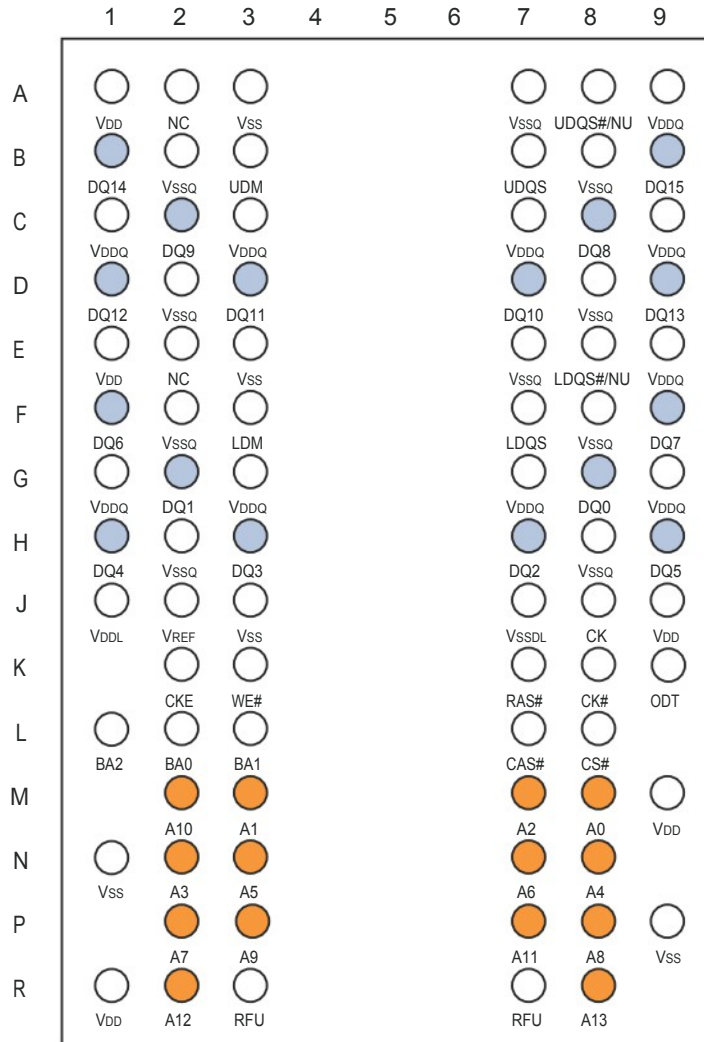


Figure 2: Package Dimensions
84-Ball FBGA Package
(9mm x 12.5mm) - x16, PK

